AMENDMENTS TO THE CLAIMS

1. (Currently amended) A process for controlling a PMC memory component, comprising:

sending out a signal to select one of several modes for the PMC memory component; and

operating the PMC memory component in accordance with the specific mode selected by the signal, wherein depending on the specific mode selected, a PMC memory cell of the PMC memory component is brought into states of different storage permanence by correspondingly selecting a height of a current ~~intensity~~ of a programming pulse applied to the PMC memory cell.

2. (Previously presented) The process of claim 1, further comprising

writing data into the memory component in accordance with the specific mode selected by the signal.

3. (Previously presented) The process of claim 2, whereby one of the modes is a soft writing mode.

4. (Previously presented) The process of claim 2, whereby one of the modes is a non-volatile writing mode.

5. (Previously presented) The process of claim 2, whereby one of the modes is a hard writing mode.

6. (Previously presented) The process of claim 2, whereby for the writing of data into the memory component, a current intensity, a duration of a programming pulse is adapted, and/or a number of programming pulses.

7. (Original) The process of claim 1, whereby the memory component comprises PMC memory cells.

8. (Original) The process of claim 1, whereby the signal is sent out over one or several separate mode selection lines.

9. (Original) The process of claim 1, whereby the signal is sent out over the same line as actual data to be stored in the memory component.

10. (Previously presented) The process of claim 9, whereby the signal is sent out over the line by use of memory mode selection bits, the bits being followed by bits carrying the data to be stored in the memory component.

11. (Currently amended) A memory system, comprising:

a memory component; and

a controller adapted to operate the memory component in several different modes by bringing a memory cell of the memory component into states of different storage permanence by correspondingly ~~selected~~ selecting a height of a current ~~intensity~~ of a programming pulse applied to the memory cell.

12. (Previously presented) The system of claim 11, whereby one of the modes is a soft writing mode.

13. (Previously presented) The system of claim 11, whereby one of the modes is a non-volatile writing mode.

14. (Previously presented) The system of claim 11, whereby one of the modes is a hard writing mode.

15. (Original) The system of claim 11, whereby the memory component comprises PMC memory cells.

16. (Currently amended) A process for controlling a PMC memory component, comprising:

sending out a signal to select one of several modes for the PMC memory component; and

operating the PMC memory component in accordance with the mode selected by the signal, wherein depending on the mode selected a PMC memory cell of the PMC memory component is brought into states of different storage permanence by correspondingly selecting a duration of a programming pulse applied to the PMC memory cell.

17. (Canceled)

18. (Currently amended) A memory system, comprising:

a memory component; and

a controller adapted to operate the memory component in several different modes by bringing the memory component into states of different storage permanence by correspondingly selecting a duration of a programming pulse applied to the memory cell.

19. (Canceled)